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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/633,606 07/31/2003		07/31/2003	Steven Moore	30287-94	5162		
44279	7590	02/06/2006		EXAMINER			
PULSE-LI	•		DESCHERE, ANDREW M				
1969 KELL CARLSBA		=	ART UNIT	PAPER NUMBER			
			2836				

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application	on No.	Applicant(s)					
		10/633,60)6	MOORE ET AL.	A				
Office Action Summary		Examiner	,	Art Unit	— Co				
		Andrew M	. Deschere	2836					
Period fo	The MAILING DATE of this communica or. Reply	ition appears on the	cover sheet with	the correspondence addre	:ss				
WHIC - Exter after - If NO - Failu Any	ORTENED STATUTORY PERIOD FOR CHEVER IS LONGER, FROM THE MAIL asions of time may be available under the provisions of 3 SIX (6) MONTHS from the mailing date of this community or to reply within the set or extended period for reply will reply received by the Office later than three months after ad patent term adjustment. See 37 CFR 1.704(b).	LING DATE OF TH 37 CFR 1.136(a). In no evolution. ory period will apply and will, by statute, cause the app	HIS COMMUNICA ent, however, may a rep ill expire SIX (6) MONTH lication to become ABAI	ATION. Ily be timely filed Is from the mailing date of this comm NDONED (35 U.S.C. § 133).					
Status									
1)	Responsive to communication(s) filed	on							
<i>,</i> —	This action is FINAL. 2b)⊠ This action is non-final.								
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is								
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
5)	Claim(s) <u>1-55</u> is/are pending in the app 4a) Of the above claim(s) is/are Claim(s) is/are allowed. Claim(s) <u>1-55</u> is/are rejected.		nsideration.						
	Claim(s) is/are objected to.								
•	Claim(s) are subject to restrictio	on and/or election r	equirement.						
Applicati	on Papers								
	The specification is objected to by the E	Examiner.							
•	The drawing(s) filed on 31 July 2003 is/		d or b)⊠ object∈	ed to by the Examiner.					
	Applicant may not request that any objection	on to the drawing(s) t	e held in abeyanc	e. See 37 CFR 1.85(a).					
11)	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority u	ınder 35 U.S.C. § 119								
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).									
* 5	See the attached detailed Office action f	for a list of the certi	fied copies not re	eceived.					
Attachmen	t(s)								
1) Notic	e of References Cited (PTO-892)			mmary (PTO-413)					
3) 🔯 Infon	te of Draftsperson's Patent Drawing Review (PTO mation Disclosure Statement(s) (PTO-1449 or PT or No(s)/Mail Date 7/31/2003.			Mail Date ormal Patent Application (PTO-15 	52)				

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DETAILED ACTION

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer <u>cannot</u> overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 54 and 55 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of the following claims:

- Claims 25 and 26 of copending Application No. 10/633,608.
- Claims 41 and 42 of copending Application No. 10/723,562.
- Claims 1 and 2 of copending Application No. 11/126,446.

This is a <u>provisional</u> double patenting rejection since the conflicting claims have not in fact been patented.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Page 5, line 18 of the specification states, "Another example of a conventional radio frequency technology is illustrated in FIG. 1." See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per

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37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Figure 3 does not contain reference number 30, as found in the specification on page 15, line 9. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-x rejected under 35 U.S.C. 102(e) as being anticipated by United States

Patent 6,433,720, issued to Libove et al. (hereafter referred to as "Libove").

Libove discloses a pulse generating circuit with a control input (Figure 1, Control), a first input stage (Input), a plurality of switching elements (transistors Q_N) responsive to a first voltage level (V₁) and a second voltage level (V₂), wherein the control input provides a transition signal from the first voltage level to the second voltage level (column 3, lines 18-53; claim 1). With its use in complex communication systems (column 2, lines 40-48) a microprocessor (such as that seen in Figure 8) will provide the control signal. The input stage is formed by a differential pair (Q₁ and Q₂), and the first voltage level is greater than the second voltage level (claim 2). The switching elements may be formed by differentially paired transistors (Figures 1 and 2) or differentially paired diodes (Figures 4 and 5). The voltage levels in the circuit will be lower than five volts (column 5, lines 41-43; column 3, lines 26-35). The pulses of the invention may be of arbitrary duration (column 6, lines 46-63).

Claims 20-26 and 28 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Libove.

Libove discloses a pulse generation circuit with four transistor pairs (see claim 6 and Figure 1 of Libove). The first pair has its control (gate) terminals connected to input terminals, and its source terminals connected to a current source. The second pair has its control (gate) terminals connected to a first voltage level, and its source terminals connected to the drain terminals of the first pair. The third pair has its control (gate) terminals connected to a control signal and its source terminals connected to the drain terminals of the second pair. The fourth pair has its control (gate) terminals connected to a third voltage level, its source terminals connected to the drain terminals of the third

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pair, and its drain terminals connected to a differential output. A first resistor and a second resistor have a first terminal coupled to a power supply and a second terminal connected to the drain terminals of the fourth transistor pair. A microprocessor and digital to analog converter is attached to the circuit (see Figure 8 of Libove).

With respect to claim 21, Libove discloses that the second, third, and fourth transistor pairs are responsive to the first voltage level, the third voltage level, and the control signal (see claim 7 of Libove).

With respect to claim 22, Libove discloses that the digital to analog converters are connected to and controlled by the microprocessor (Figure 8 of Libove).

With respect to claim 23, Libove discloses that the control signal causes the circuit to generate a pulse when the control signal is between the first voltage level and the third voltage level (see claim 8 of Libove).

With respect to claim 24, Libove discloses a capacitor coupled to the differential output (see claim 10 of Libove).

With respect to claim 25, Libove discloses a fifth pair of differential transistors with control (gate) terminals connected to the control signal, and source terminals connected to the drain terminals of the third transistor pair and the source terminals of the fourth transistor pair (see claim 11 of Libove).

With respect to claim 26, Libove discloses a sixth transistor pair with control (gate) terminals connected to a second voltage level, source terminals connected to drain terminals of the second transistor pair, and drain terminals connected to the power supply (see claim 12 of Libove).

With respect to claim 28, Libove discloses in claim 13 varieties of transistors that may be used in the differential transistor pairs; this group is identical to that of claim 28 in the present application.

Claims 13-19 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Libove. Claims 13-19 of the application are rejected similarly as above to claims 20-26 and 28 of the application. Claims 13-19 are rejected with respect to claims 1-5 of Libove, and Figure 8 of Libove. Figure 8 of Libove shows a microprocessor and digital to analog converter is attached to the circuit.

Claims 39-43 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Libove. Claims 39-43 of the application are rejected similarly as above to claims 20-26 and 28 of the application. Claims 39-43 are rejected with respect to claims 27-30 of Libove, and Figure 8 of Libove. Figure 8 of Libove shows a microprocessor and digital to analog converter is attached to the circuit.

Claims 44-47 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Libove. Claims 44-47 of the application are rejected similarly as above to claims 20-26 and 28 of the application. Claims 44-47 are rejected with respect to claims 31-33 of Libove, and Figure 8 of Libove. Figure 8 of Libove shows a microprocessor and digital to analog converter is attached to the circuit.

Claims 48-53 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Libove. Claims 48-53 of the application are rejected similarly as above to claims 20-26 and 28 of the application. Claims 48-53 are rejected with respect to claims 34-39 of Libove, and Figure 8 of Libove. Figure 8 of Libove shows a microprocessor and digital to analog converter is attached to the circuit.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Libove and United States Patent 5,798,661, issued to Runaldue et al. (hereafter referred to as "Runaldue").

While Libove discloses a pulse generation circuit with data inputs, switching elements, set voltage levels, and an aggregated waveform (Figure 9), there is no explicit teaching to use a sinusoidal waveform. However, the use of a sinusoidal output in such a system is well known in the art, as taught by Runaldue. Runaldue teaches a system for continuous waveform synthesis that generates sinusoidal waveform pulses for transmission (system shown in Figure 1, output waveforms in Figures 2a-2h). It would have been obvious to one of ordinary skill in the art at the time of the invention to aggregate the pulses of the system of Libove into a sinusoidal waveform for communication over a transmission line.

Claims 27, 29-35, and 37-38 rejected under 35 U.S.C. 103(a) as being unpatentable over Libove and United States Patent Application Publication 2004/0190597 (hereafter referred to as "Cowie").

Libove discloses a pulse generation system with a control means, aggregating means, a microprocessor, and digital to analog converters (Figures 1, 8, and 10).

Pulses are generated in response to voltage transitions by parallel-connected pulse

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generators. However, Libove does not explicitly disclose the use of a demultiplexor.

Cowie teaches a pulse communication system that utilizes a demultiplexor. It would have been obvious to one of ordinary skill in the art at the time of the invention to integrate a demultiplexor into the invention of Libove to break down a stream of high-rate data at the input of the system so that a lower data rate may be transmitted.

Claim 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Libove, Cowie, and United States Patent 6,057,949, issued to Kinstler (hereafter referred to as "Kinstler").

A combination of Libove and Cowie provides a pulse generation system with demultiplexing means. However, this combination teaches the use of pulse generating means connected in parallel and provides no provision for a series connection. Kinstler teaches an infrared communications system that has pulse generators in series connection (Figure 2, column 4, lines 39-49). It would have been obvious to one of ordinary skill in the art at the time of the invention to provide pulse generators in series in the combination of Libove and Cowie to adapt the system for bidirectional infrared communications.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure--

United States Patent 4,179,733, issued to Launzel et al. discloses computer control of communication signals, including digital to analog conversion.

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United States Patent Application Publication 2005/0068932 ("Lakkis") discloses an ultra-wideband communication system, including discrete pulses transmitted on sinusoidal waveforms.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew M. Deschere whose telephone number is (571) 272-8391. The examiner can normally be reached on M-F 8:30-6:00, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMD

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